PARASITIC RESISTANCE EXTRACTION ERRORS WITH IMPLICATIONS FOR FET MODEL ACCURACY AROUND $V_{ds} = 0$

Vicentiu I. Cojocaru and Thomas J. Brazil

Department of Electronic and Electrical Engineering
University College Dublin, Dublin 4, Ireland.

ABSTRACT

The accuracy of non-linear FET models around the origin in the V_{gs} - V_{ds} bias plane, may be seriously affected by errors in the extracted values of the source and drain parasitic resistances. In this paper we present test results that prove how relatively small errors of this kind, which can be easily encountered when using conventional extraction techniques, can lead to large errors in the values extracted for some intrinsic parameters, and in particular for the two gate capacitances. The source of these errors is investigated and, as a solution, an improved extraction methodology is offered, which substantially reduces the risk of such errors.

INTRODUCTION

Parameter extraction of equivalent circuit non-linear models for microwave FETs, has been an area well covered by researchers over the years and it is fair to say that in some respects it has reached a certain level of maturity. There have been several approaches proposed in relation to the extraction of the parasitic elements [1-4], most of them based on a combination of DC and small-signal S-parameters measured under certain special bias conditions. As far as the de-embedding of parasitics and the extraction of the intrinsic elements is concerned, the very elegant method proposed by Dambrine *et al.* [1], and further improved by Berroth and Bosch [2], is well established and very efficient. It is, however, interesting that many device manufacturers still complain about serious problems and inconsistencies when these extraction techniques are applied in practice. One important and persistent complaint regards the frequently-observed presence of large asymmetries between the gate-to-source and gate-to-drain capacitances extracted at $V_{ds}=0$. This is in sharp contrast to the relative symmetrical geometry presented by the large majority of FET devices, under these particular bias conditions. The consequences can be very serious from a modelling point of view, and designs based on these models can be badly affected, especially in applications such as mixers and switches.

In this paper we investigate possible causes for such errors in the parameter extraction process, their impact on the extracted multi-bias intrinsic elements and the non-linear models built upon those values and solutions to prevent them. On the basis of several tests carried out on both MESFET and PHEMT devices (of various sizes), we establish that even small mutual errors in the values extracted for the source and drain parasitic resistances, can cause quite significant asymmetries in the extracted values for the gate capacitances at $V_{ds} = 0$ (and to a greater or lesser extent, for the other intrinsic elements of the equivalent circuit model as well). Moreover, these extracted capacitance values are affected not only at $V_{ds} = 0$, but also in the linear operation region of the devices ($V_{ds} < V_{ds,sat}$). Also, the asymmetry increases in magnitude starting from the pinch-off, towards the forward gate-bias region. We outline the most important points of an extraction methodology that has been implemented in order to avoid such errors and finally, we present comparative test results for both MESFET and PHEMT devices, to prove its success.

POSSIBLE ERRORS IN THE EXTRACTION OF PARASITIC RESISTANCES

Most of the techniques employed to extract the parasitic elements of a microwave FET, are based upon small-signal S-data or DC data, measured at $V_{ds} = 0$. The main reason is that under these conditions the equivalent circuit model can be simplified to a great extent. Furthermore, one of the factors which allows this simplification, is the relative symmetry of the active channel under these bias conditions, determined mainly by the symmetry of the depletion region under the gate. The small geometrical asymmetries that exist normally between the source and drain contacts relative to the gate, are not likely to have a significant impact in this case. The circuit topologies commonly used for parasitic extraction normally differ

0-7803-4603-6/97/$5.00 (c) IEEE

between the "below pinch-off" case (Fig. 1.a) and the "above pinch-off" case (Fig. 1.b).

Although perhaps more convenient, there are a couple of disadvantages associated with the second topology:
i) it is not consistent with the topology used in all the other circumstances (below pinch-off and under normal bias conditions), which involves two gate capacitances;
ii) it carries with it an uncertainty related to the balance between the two channel resistances, R_{chs} and R_{chd}.

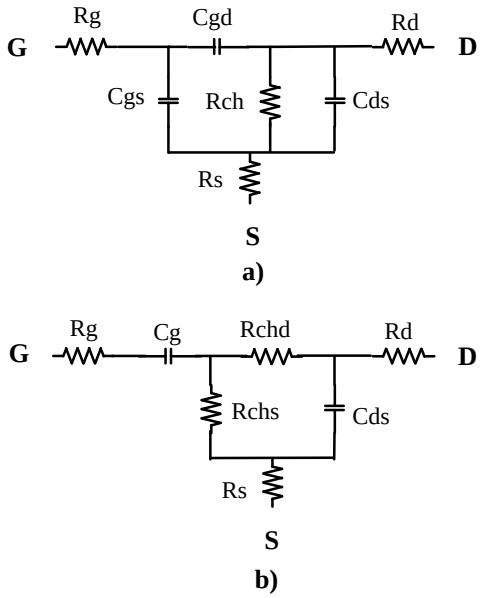


Figure 1. Simplified equivalent circuit topologies used for parasistic extraction; a) "below pinch-off" case; b) "above pinch-off" case.

The partitioning rule for these resistances is normally chosen as follows:

$$R_{chs} = \alpha R_{ch}\ ; \qquad R_{chd} = (1-\alpha)\, R_{ch}; \tag{1}$$

where R_{ch} is the total channel resistance and α has a value that varies, from author to author, between 0.33 to 0.5. It is quite obvious that if the balance between those two resistances (i.e. the value of α) is incorrect, the values determined for the source and drain resistances will be affected.

THE IMPACT ON THE EXTRACTION OF INTRINSIC ELEMENTS

The impact that even relatively small errors in the values for R_s and R_d, have upon the extracted values of the intrinsic gate capacitances, is surprisingly high. We carried out tests on two FET foundry devices (one MESFET from *GEC-Marconi*, and one PHEMT from *Philips*), and the results for $V_{ds} = 0$, are shown in Fig. 3, for the MESFET and in Fig. 4, for the PHEMT. The equivalent circuit topology used for the extraction is the one shown in Fig. 2, and the methodology used is more or less the one presented in [3].

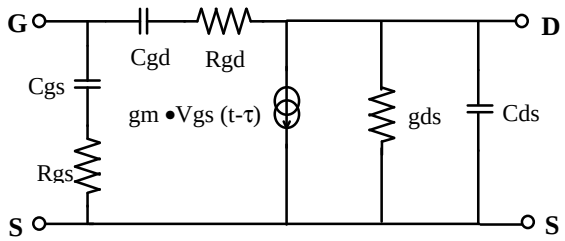


Figure 2. Small-signal equivalent circuit model of the intrinsic FET

The graphs represent two different situations: a) the correct values for R_s and R_d are used (determined via the methodology described further in this paper), and as a result, the two gate capacitances are almost identical; b) the two resistance values have been slightly altered, and as a result the two capacitances follow very different patterns above the pinch-off. Other interesting observations made during these tests are:

- the magnitude of the difference between the two capacitances is closely related to the alteration of the difference between R_s and R_d, and does not depend too much on the absolute values of the resistances (within reasonable limits, of course); if the value of $(R_s\text{-}R_d)$ moves very far away from the correct one, the extracted capacitances can go totally out of range;
- the sense in which this difference between C_{gs} and C_{gd} occurs, depends on the sense in which the absolute value of $(R_s\text{-}R_d)$ is changing relative to the correct value;
- below pinch-off the two capacitances are always equal, the differentiation appears only above pinch-off and increases progressively towards forward gate-bias region;
- the difference between the two capacitances is also observed within the linear operation region of the devices $(0<V_{ds}<V_{ds,sat})$; C_{gs} and C_{gd} tend to converge progressively towards the correct values around $V_{ds,sat}$. In the saturation region these phenomena are no longer observed;
- the values extracted for the two charging resistances, are also affected to a certain extent, but the other elements in the equivalent circuit (Fig. 2) seem to be only slightly affected. Overall, the largest influence appears to be that seen on the two gate capacitances.

These phenomena are hidden below pinch-off and in the saturation region, by the very high resistance exhibited between the intrinsic drain and source. Above pinch-off, when the channel opens and in the linear operating region the active channel resistance is of the same order of magnitude as the parasitic and charging resistances.

IMPROVED PARAMETER EXTRACTION STRATEGY

(1) The parasitic resistances are determined using solely the "unbiased" and "pinched-off" FET S-data. The same "PI" topology (Fig. 1.a) is used to model the FET in both these bias conditions. For low enough frequencies (f < 10GHz, where $\omega\ R_{ch}\ C << 1$), the "PI" structure C_{gs}-C_{gd}-R_{ch} can be related to the "T" structure C_g-R_{chs}-R_{chd} by comparing the input and output **Z** parameters of the two configurations. From eqs. (2), (3) (below), we deduce:

$$C_g = C_{gs} + C_{gd} = 2\ C_{gs}; \quad R_{chs} = 0.25\ R_{ch};$$

$$R_{chd} = 0.75\ R_{ch} \quad (\alpha = 0.25) \tag{4}$$

With this value for α, we can use now the "T" topology (Fig.1.b) and the technique described in [3] to determine R_s and R_d. Another very important aspect is the frequency range where the extraction of R_g, R_s and R_d is carried out. The frequency dependance of these elements should be monitored, since it tends to vary from device to device. The frequency range should be chosen so that the impact of inductive and/or capacitive reactances in the circuit is minimum.

(2) The intrinsic elements are extracted, using an equivalent circuit model as shown in Fig. 2, with both charging resistances, R_{gs} and R_{gd}, included, and using the technique described in [2]. Again, the frequency range where the extraction is carried out is very important, and different frequency ranges might be needed to extract different parameters. The results when such a methodology is used, are seen in Fig. 3 and Fig. 4, giving the clear result that the two gate capacitances are identical.

CONCLUSIONS

We have demonstrated that rather small alterations in the values determined for the source and drain parasitic resistances can have serious repercussions on the values extracted for the two gate capacitances, at $V_{ds} = 0$ and in the linear operation region. Test results for both MESFET and PHEMT foundry devices, show errors reaching over 50% in the values of C_{gs} and C_{gd}, when small adjustments are made to R_s and R_d. Weaknesses in most of the commonly used extraction procedures are proven to be the cause of such errors. These inaccuracies can have severe repercussions on the quality of FET models built upon such faulty values, particularly when they are used in applications such as mixers and switches, when the devices are operated mainly in the most affected bias regions. Finally, we have outlined an improved extraction methodology, to reduce the probability of such errors.

$$Z_{11T} = R_{chs} - j\cdot\left(\frac{1}{\omega\cdot C_g}\right)$$
$$Z_{22T} = R_{chs} + R_{chd} \tag{2}$$

$$Z_{11\Pi} = \frac{\frac{1}{j\cdot\omega\cdot C_{gs}}\cdot\left(R_{ch} + \frac{1}{j\cdot\omega\cdot C_{gs}}\right)}{R_{ch} + \frac{2}{j\cdot\omega\cdot C_{gs}}} = \frac{\frac{R_{ch}}{\omega^2\cdot {C_{gs}}^2} - j\cdot\left(\frac{{R_{ch}}^2}{\omega\cdot C_{gs}} + \frac{2}{\omega^3\cdot {C_{gs}}^3}\right)}{{R_{ch}}^2 + \frac{4}{\omega^2\cdot {C_{gs}}^2}} \cong \frac{R_{ch}}{4} - j\cdot\frac{1}{\omega\cdot(2\cdot C_{gs})}$$

$$Z_{22\Pi} = \frac{R_{ch}\cdot\left(j\cdot\frac{2}{\omega\cdot C_{gs}}\right)}{R_{ch} + j\cdot\frac{2}{\omega\cdot C_{gs}}} = \frac{R_{ch}\cdot\frac{4}{\omega^2\cdot {C_{gs}}^2} + j\cdot {R_{ch}}^2\cdot\frac{2}{\omega\cdot C_{gs}}}{{R_{ch}}^2 + \frac{4}{\omega^2\cdot {C_{gs}}^2}} \cong R_{ch} + j\cdot R_{ch}\cdot\omega\cdot(2\cdot C_{gs}) \cong R_{ch} \tag{3}$$

AKNOWLEDGEMENTS

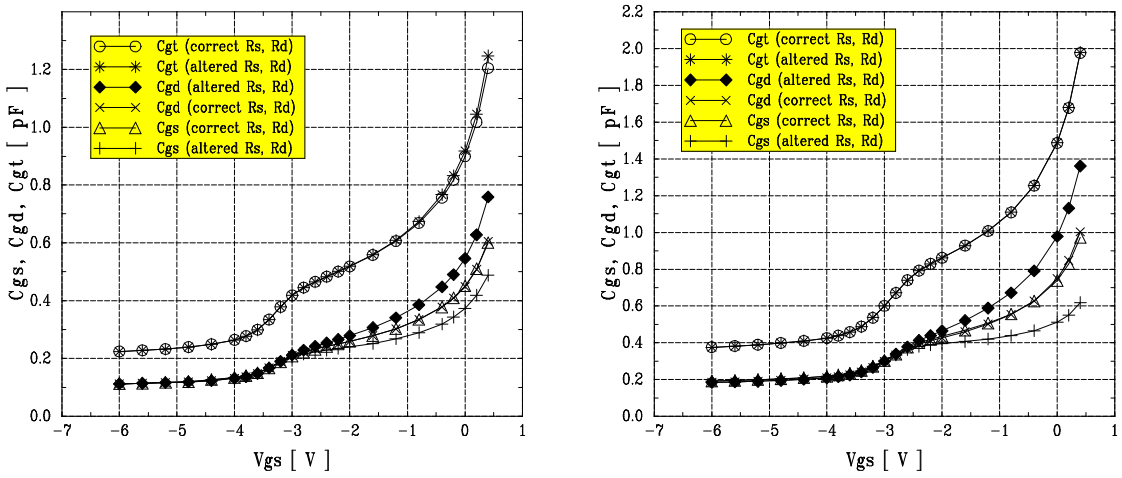
This work has been partly supported by the ESPRIT-EDGE project. The authors would like to thank Remy Leblanc of Philips Microwave Limeil and Mike Brookbanks of GEC Marconi, for useful discussions during this work.

REFERENCES

[1] Dambrine G., Cappy A., Heliodore F., Playez E., "A new method for determining the FET small-signal equivalent circuit", *IEEE Trans. Microwave Theory and Tech.*, Vol. 36, no.7, pp.1151-1159, July 1988.

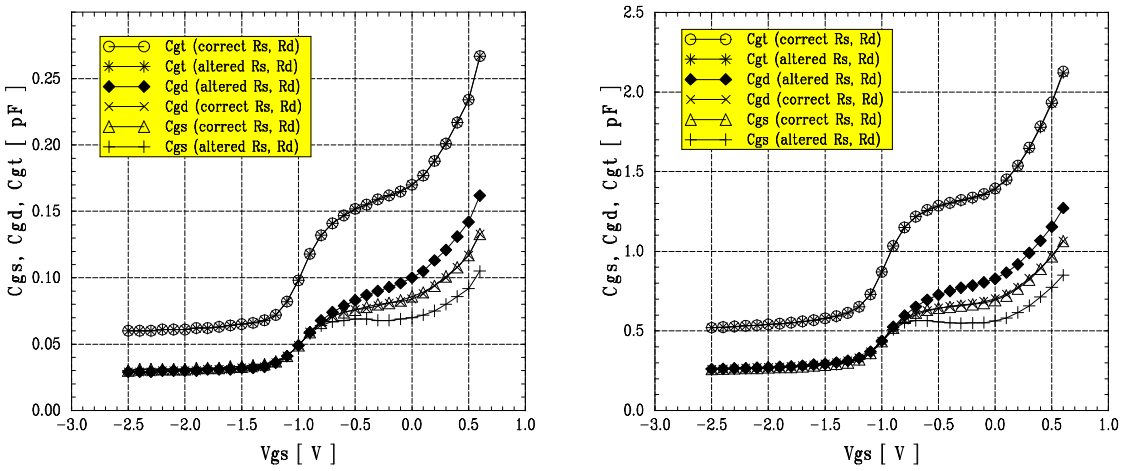
[2] Berroth M., Bosch R., "Broad-band determination of the FET small-signal equivalent circuit", *IEEE Trans. on Microwave*

Theory and Tech., Vol.38, pp.891-895, July 1990.
[3] Cojocaru V.I., Brazil T. J., "A large-signal model for MESFET's and HEMT's valid at multiple DC bias points ", *Proc. of GAAS'94*, pp.419-422, Turin, 1994.
[4] Tayrani R., Gerber J.E., Daniel T., Pengelly R.S., Rhode U.L., "A new and reliable direct extraction method for MESFETs and HEMTs", *Proceedings of the 23rd EuMC*, pp. 451, Madrid, 1993.



a) **b)**

Figure 3. a) Extracted gate capacitances at $V_{ds} = 0$, for a 720µm MESFET for two sets of values for R_s and R_d. In the first case, with the values extracted using the improved methodology outlined in this paper, it is seen how the two gate capacitances are essentially identical, as required. In the second case, the value of R_d has been altered from 1.3 to 1.8 ohms, and the capacitance extraction has been repeated. The results show major differences between the two gate capacitances above pinch-off ; **b)** Similar test for a 1200µm MESFET (R_d has been altered from 0.79 to 1.2 ohms).



a) **b)**

Figure 4. a) Similar test as in Fig. 3, repeated for a 120µm PHEMT (R_d has been altered from 4.72 to 5.2 ohms) **b)** Results for a 1200µm PHEMT (R_d has been altered from 0.43 to 0.8 ohms).